UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/512,149	02/23/2000	Vishnu K Agarwal	MI22-1322	3457

21567 7590 04/20/2005

WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
PIZARRO CRESPO, MARCOS D	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/512,149	AGARWAL, VISHNU K	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-14,56-70 and 72-108* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,4-14,56-70,72-82,90-98 and 104* is/are allowed.

6)☒ Claim(s) *83,86-89,99-103 and 105-108* is/are rejected.

7)☒ Claim(s) *84 and 85* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Attorney's Docket Number: MI22-1322
Filing Date: 2/23/2000
Claimed Foreign Priority Date: none
Applicant(s): Agarwal
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on 2/16/2005.

Acknowledgment

1. The amendment filed on 2/16/2005, responding to the Office action mailed on 11/16/2004, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1, 4-14, 56-70, and 72-108.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 83, 86-89, 99, 101, 102, and 105 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele (US 5760474) in view of Ramakrishnan (US 5192871).

4. Regarding claim 83, Schuele (see, *e.g.*, fig. 6) shows most aspects of the instant invention including an integrated circuitry comprising:

- A substrate **30**
- An insulative material **37** formed over the substrate **30**
- An opening formed in the insulative material **37**
- A capacitor **75** comprising:
  - A first electrode layer **50** formed within the opening
  - A dielectric region **60** formed over the first electrode layer **50** and within the opening
  - A second electrode layer **70** formed over the dielectric region **60**

Schuele, however, fails to show that the dielectric region is formed of a high-K material comprising a crystalline portion and an amorphous portion. Ramakrishnan, on the other hand, teaches that it would be highly advantageous for Schuele's dielectric region to comprise a high-K dielectric material having a crystalline portion and an amorphous portion. This structure would provide the sought-after high-dielectric constant that characterizes crystalline dielectric materials, and at the same time would prevent the migration of foreign materials that may adversely affect the dielectric constant of the capacitor dielectric layer. See, *e.g.*, Ramakrishnan, col.1/ll.45-50, col.32/ll.35-37, and col.3/ll.23-30.

It would have been obvious at the time of the invention to one of ordinary skill in the art to have a high-K dielectric material having a crystalline portion and an amorphous portion for the capacitor dielectric region of Schuele, as suggested by Ramakrishnan, to protect the dielectric properties of the layer.

5. Regarding claim 86, Ramakrishnan (see, *e.g.*, col.2/ll.50-52) shows the portion of the amorphous material comprising at least 70% amorphous phase.

6. Regarding claim 87, Ramakrishnan shows that the high-K dielectric layer may comprise Ta_2O_5 (see, *e.g.*, col.3/ll.53).

7. Regarding claim 88, Ramakrishnan (see, *e.g.*, col.2/ll.50-52) shows the portion of the amorphous material comprising greater than 90% amorphous phase.

8. Regarding claim 89, Ramakrishnan shows that the portions of amorphous and crystalline materials may be from different materials (see, *e.g.*, col.2/ll.48).

9. Regarding claim 99, Ramakrishnan teaches that the amorphous material is provided in an amount effective to reduce leakage current through the crystalline material (see, *e.g.*, col.2/ll.68-col.3/ll.3).

10. Regarding claims 101 and 102, Schuele shows that the capacitor comprising a portion of a DRAM circuitry.

11. Regarding claim 105, Ramakrishnan shows the dielectric layer comprising another portion, which comprises dielectric material (see, *e.g.*, fig. 3).

12. Claim 100 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele/Ramakrishnan in view of Wu (US 5998247).

13. Regarding claim 100, Schuele/Ramakrishnan shows most aspects of the instant invention (see, e.g., paragraph 9 above with respect to claim 83). They also teach that a DRAM includes a capacitor **75** (see, *e.g.*, Schuele/fig. 6). However, they fail show the capacitor also comprising a portion of a logic circuitry. Wu (see, *e.g.*, col.1/ll.12-15), on

the other hand, teaches that logic circuits with DRAM devices are demanded as high-performance devices that reduce power consumption and increase packing density.

It would have been obvious at the time of the invention to one of ordinary skill in the art to include the capacitor of Schuele/Ramakrishnan into a logic circuit, as suggested by Wu, to reduce power consumption.

14. Claims 103 and 106-108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele/Ramakrishnan in view of Venkatraman (US 6093966), Chen (US 6100137) and Yu (US 6274443).

15. Regarding claims 103 and 106-108, Schuele/Ramakrishnan shows most aspect of the instant invention (see, *e.g.*, paragraph 9 above with respect to claim 83). They, however, fail to show the outermost portion of the insulating material comprising an antireflective coating layer made of SiON. Venkatraman (see, *e.g.*, col.4/ll.54-59), on the other hand, teaches that providing Schuele/Ramakrishnan's outermost portion of the insulating material with an antireflective layer would minimize the reflections from underlying features during the definition of the opening so that a uniform distribution of the critical dimensions of the opening is obtained. Yu (see, *e.g.*, col.5/ll.2-3, col.15/ll.44-47) teaches that one of the most commonly used ARC is SiON, which enhances the imaging effect in photolithographic processing. Chen (see, *e.g.*, col.2/ll.15-25) further teaches that a SiON layer would provide the outermost portion of the insulating material of Schuele/Ramakrishnan with an improved antireflective coating.

It would have been obvious at the time of the invention to one of ordinary skill in the art to provide Schuele/Ramakrishnan's outermost portion of the insulating material

with a SiON antireflective layer, as suggested by Venkatraman/Yu/Chen, so that a uniform distribution of the critical dimensions of the opening is obtained.

Allowable Subject Matter

16. Claims 1, 4-14, 56-70, 72-82, 90-98, and 104 are allowed.

17. Claims 84 and 85 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

18. The applicants argue:

> Schuele provides extensive teachings to provide a barrier layer to prevent migration of materials. See, e.g., Schuele at: col.3/ll.1-15, 40-60, col.4/ll.54-67, col.5/ll.40-55, abstract, and background. The examiner now suggests that Schuele provides a barrier layer to prevent diffusion only between the capacitor lower electrode and the capacitor dielectric layer and tacitly states that Schuele fails to teach to provide a barrier layer to prevent diffusion between the top capacitor electrode and the capacitor dielectric layer. Accordingly, the examiner relies on Ramakrishnan to provide an amorphous capacitor dielectric layer to prevent diffusion between the top electrode and the dielectric layer. This alleged motivation is, however, redundant since Schuele teaches that the dielectric layer 60 is to be annealed to prevent diffusion of foreign materials between the upper electrode and the ferroelectric layer (see, *e.g.*, Schuele at: col.4/ll.56-60). Accordingly, there is no motivation to combine Schuele with Ramakrishnan and claim 83 is, therefore, allowable.

The examiner responds:

In all the sections that the applicants quoted above, Schuele uses a barrier layer to prevent diffusion of silicon from the plug to the capacitor lower electrode and from the lower electrode to the dielectric layer, and to prevent oxidation of the plug when annealing the dielectric layer as described in col.4/ll.56-60 (see, *e.g.*, col.1/ll.60-67). Ramakrishnan, on the other hand, uses the amorphous portion of the dielectric layer *inter alia* to prevent the inclusion of foreign materials form layers located above the dielectric layer, *e.g.*, from the top electrode to the capacitor dielectric region.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 872-9306**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

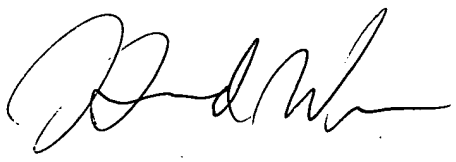
22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the

examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

23. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

24. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/310, 438/240, 361/313	11/10/2004
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	11/10/2004



Marcos D. Pizarro-Crespo
Patent Examiner, Art Unit 2814
Art Unit 2814
571-272-1716
marcos.pizarro@uspto.gov
MDP/mdp 3/4/2003

Howard Weiss
Primary Examiner
Art Unit 2814